AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph commencing at page 9, line 15 as follows:

In this embodiment, ~~the components disclosed in Claims are realized as follows:~~ the image sensing apparatus is realized as an electronic still camera; the image quality mode setting block is realized as a part of the function of a CPU 14 and mode selector switch 19; the solid state image sensing element is realized as a CCD 4; the AD conversion block is realized as an AD converter 8; the digital signal processing block is realized as a digital signal processing circuit 9; the data thinning block is realized as a part of the function of an LCD driver 11; the image storage block is realized as a part of the function of the CPU 14, a frame memory 10, an interface circuit 12, and a recording medium 16; the image display block is realized by a part of the function of the CPU 14, the LCD driver 11, and an LCD 15. In addition to these basic components, other components which will be detailed later are provided.

Please amend the paragraph commencing at page 18, line 13 as follows:

Next, explanation will be given on the "PC mode" shown in Fig. ~~4 (d)~~ 4(a). This mode is used to display an image obtained by the electronic still camera, on a personal computer. Explanation will be given on a case that a user turns on the power switch, checks an object on the LCD display mode, and sets the PC display mode. It should be noted that the PC display mode can also be set without using the LCD display mode.

Please amend the paragraph commencing at page 19, line 5 as follows:

Next, explanation will be given on the reproduction mode shown in Fig. ~~4 (e)~~ 4(b). In this case, the image data to be reproduced is data which has been subjected to the signal processing of the aforementioned quality mode and stored in the recording medium 16, the frame memory 10, the personal computer hard disc, and the like. In order to read out this data and process it in the LCD driver 11 so as to be displayed, operation of those components not related to the reproduction process such as CCD 4, the analog signal processing circuit 5, the AD converter 8, and the digital signal processing circuit 9 is stopped, thereby reducing the power consumption. Accordingly, there is no need of bit modification of the AD converter 8 and the digital signal processing circuit 9.

Please amend the paragraph commencing at page 21, line 10 as follows:

This embodiment differs from the first embodiment in the following configuration. The AD converter 8 having the variable bit count is replaced by, for example, a 12-bit AD converter 20, a 10-bit AD converter 21, and an 8-bit AD converter 22. The switching circuit 23 is controlled by an AD converter selection signal 24 from the CPU 14 according to the image quality mode. When the high quality mode is selected, the AD converter 20 having the greatest quantization bit count is selected. When the standard quality mode is selected, the 10-bit AD converter 21 is selected. When the economy mode is selected, the AD converter 22 having the smallest quantization bit count is selected. In this case, the CPU 14 reads in the setting state of the switch circuit 23 and ~~modified~~ modifies the signal processing contents of the digital signal processing circuit 9 according to the bit count setting. This embodiment has

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the same effect as the first embodiment.

Please amend the paragraph commencing at page 22, line 2 as follows:

It should be noted that in the aforementioned embodiments, explanation has been given on the present invention applied to an electronic still camera but the present invention can also be applied to an image sensing apparatus other than the electronic still camera. Moreover, in the aforementioned embodiments, explanation has been given on a configuration using the LCD 15 for monitoring an object but the same effect can be obtained even when using a display apparatus other than the LCD 15. Moreover, explanation has been given on a case of the quantization bit count as 12 bits for the high quality mode, 10 bits for the standard mode, and 8 bits for the economy mode. However, other bit counts other than these can also be selected. Moreover, the bit count conversion signal 17 and the AD converter selection signal 24 output from the CPU 14 may be also be supplied via the internal bus 18. Moreover, in the aforementioned embodiments, explanation has been given on a configuration in which the output signal from the CCD 4 is subjected to an analog signal processing and then AD-converted but the ~~analog~~ signal processing may be realized by a digital signal processing circuit. Moreover, the present invention can have the aforementioned effects regardless of whether utilized for a motion picture or a still picture. Moreover, the operation sequence shown in Fig. 3 and Fig. 4 is only an example of the operation of the present invention and it is possible to apply other sequences without departing from the spirit of the present invention. Furthermore, the present invention can be embodied in combination with a conventional technique.

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